(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 645 819 A2**

(12) EUROPEAN PATENT APPLICATION

(21) Application number: **94114655.7**

(51) Int. Cl.[6]: **H01L 27/092**

(22) Date of filing: **17.09.94**

(30) Priority: **27.09.93 JP 238615/93**

(43) Date of publication of application:
29.03.95 Bulletin 95/13

(84) Designated Contracting States:
DE FR GB

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(54) Semiconductor device capable of high speed operation and being integrated with high density.

(57) In a semiconductor device including a plurality of semiconductor cells each of which has a diffusion area, a first metal layer, and a connecting portion, the first metal layer overlies whole of the diffusion area while the connecting portion covers almost whole of the diffusion area. The semiconductor device further includes a second metal layer, and first and second power supply lines. The second metal layer has an interconnecting area positioned above the semiconductor cells and an overlapping area overlapping on the first metal layer. Each of the first and the second power supply lines consists of the overlapping area. The semiconductor cells are electrically connected to each other by a third metal layer and the interconnecting area of the second metal layer.

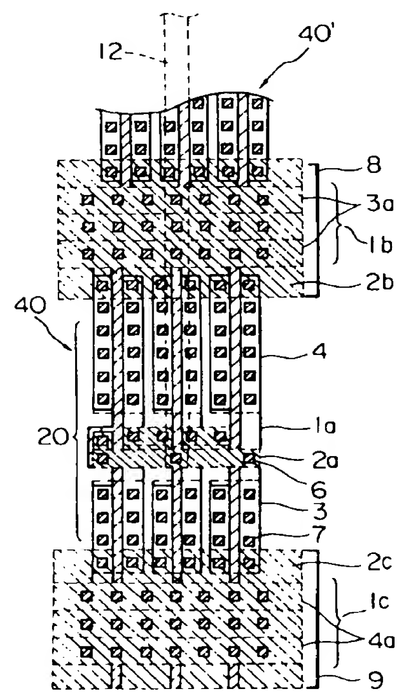


FIG. 6A

EP 0 645 819 A2

Background of the Invention:

This invention relates to a semiconductor device which comprises complementary metal oxide semiconductor (CMOS) and the like, which is for use in a semiconductor integrated circuit.

In such a semiconductor integrated circuit, a plurality of basic semiconductor cells are combined and electrically connected to each other to form a large scale logic circuit.

As will later be described more in detail, a conventional semiconductor device of the type described comprises a plurality of semiconductor cells each of which includes a diffusion area, first metal layers which form internal conductor patterns in the semiconductor cell. The first metal layers partially overlie the diffusion area. The semiconductor cell further comprises a plurality of contacts, second metal layers, first and second power supply terminals. The contacts connect the diffusion area to the first metal layers. The first and the second power supply terminals have comparatively large width and are composed of the first metal layers.

However, in the conventional semiconductor cell, wide portions of the first metal layers which define the first and the second power supply terminals partially overlie the diffusion area. It is not possible that the contacts are formed to cover almost whole of the diffusion area. As a result, a parasitic resistance of the diffusion area inevitably prevents high speed operation of the conventional semiconductor cell.

In order to make it possible that the contacts are formed to cover almost whole of the diffusion area, it should be abolished that the first metal layers which define the first and the second power supply terminals are overlapping on the diffusion area. However, when such an overlap is abolished, the conventional semiconductor cell becomes large in size, so that the conventional semiconductor device, as a whole, would also be too large in size.

Furthermore, in the conventional semiconductor device, it is necessary that patterning spaces are preserved at both sides of the semiconductor device. In other words, the second metal layers are made to be extended up to the patterning spaces at the both sides so as to electrically connect the semiconductor cells with each other. In this event, length of wiring patterns between the semiconductor cells inevitably becomes large. Therefore, the conventional semiconductor device becomes so large in size by the patterning spaces which should be preserved at the both sides. Accordingly, it becomes difficult that the conventional semiconductor devices are integrated in an IC or an LSI circuit with high density.

Summary of the Invention:

It is therefore an object of this invention to provide a semiconductor device which is operable at a high speed and which is able to be integrated with high density.

Other objects of this invention will become clear as the description proceeds.

According to an aspect of the present invention, there is provided a semiconductor device comprising: (A) a plurality of semiconductor cells each of which includes; (A1) a diffusion area; (A2) a first metal layer which overlies whole of the diffusion area and which forms internal conductor patterns; (A3) a connecting portion for connecting the diffusion area to the first metal layer; the connection portion covering almost whole of the diffusion area; (B) a second metal layer which has an interconnecting area positioned above the semiconductor cells; the first and the second metal layers having an overlapping area overlapping on each other; (C) a third metal layer; (D) first and second power supply lines each of which consists of the overlapping area; and (E) the semiconductor cells electrically connected to each other by the third metal layer and the interconnecting area of the second metal layer.

The connecting portion comprises a plurality of contacts. The connecting portion may comprise a contact covering almost whole of the diffusion area.

Brief Description of the Drawings:

Fig. 1 is a schematic plan view of a conventional semiconductor cell;

Fig. 2A is a schematic plan view of a conventional semiconductor device;

Fig. 2B is another schematic plan view of the conventional semiconductor device illustrated in Fig. 2A, in which second metal layers have not yet been provided;

Fig. 3 is a circuit diagram of a ring oscillator circuit to which the conventional semiconductor device is applied;

Fig. 4 is a schematic plan view of a semiconductor cell according to an embodiment of this invention;

Fig. 5 is a schematic sectional view of the semiconductor cell taken across A-A' illustrated in Fig. 4;

Fig. 6A is a schematic plan view of a semiconductor device according to an embodiment of this invention; and

Fig. 6B is another schematic plan view of the semiconductor device illustrated in Fig. 6A, in which second metal layers have not yet been provided.

Description of the Preferred Embodiment:

Referring to Figs. 1 to 3, conventional semiconductor cell and device will first be described for a better understanding of this invention.

In Fig. 1, illustration is made about an inverter cell, as an example of the conventional semiconductor cell.

The inverter cell comprises an n-channel area 3, a p-channel area 4, first metal layers 1a, 1b, and 1c each of which forms an internal conductor pattern in the inverter cell. The first metal layer 1b partially overlies the p-channel area 4 while the first metal layer 1c partially overlies the n-channel area 3. The inverter cell further comprises a plurality of contact holes 7, a second metal layer 2, first and second power supply terminals 8 and 9. The contact holes 7 connect the n-channel and the p-channel areas 3 and 4 to the first metal layers 1c and 1b, respectively.

As illustrated in Fig. 1, the diffusion area of the n-channel area 3 constructing an N-type MOS transistor is positioned at one side (namely, at a lower side of a sheet of Fig. 1) while the diffusion area of the p-channel area 4 constructing a P-type MOS transistor is positioned at the other side (namely, at an upper side of a sheet of Fig. 1). The first and the second power supply terminals 8 and 9 have comparatively large width and are composed of the first metal layers 1b and 1c, respectively. In the illustrated example, the first and the second power supply terminals 8 and 9 provide a power supply and a ground, respectively. Besides, an N-type area 3a serves as a contact area connected to a well (not shown) while a P-type area 4a serves as a contact area connected to a substrate (not shown). Furthermore, the first metal layer 1a (shown by real lines in Fig. 1) and the second metal layer 2 (shown by broken lines in Fig. 1) are overlapping on each other in the plan view of Fig. 1. A through-hole 6 is for use in connecting the first metal layer 1a with the second metal layer 2. An output terminal of the inverter cell is composed of the second metal layer 2.

However, in the conventional semiconductor cell mentioned with respect to the inverter cell, wide portions of the first metal layers 1b and 1c which define the first and the second power supply terminals 8 and 9 partially overlie the diffusion areas of the p-channel area 4 and the n-channel area 3. It is not possible that the contact holes 7 are formed to cover almost whole areas of the p-channel area 4 and the n-channel area 3. As a result, a parasitic resistance of the diffusion areas inevitably prevents high speed operation of the conventional semiconductor cell.

In order to make it possible that the contact holes 7 are formed to cover almost whole areas of the p-channel area 4 and the n-channel area 3, it should be abolished that the first metal layers 1b and 1c which define the first and the second power supply terminals 8 and 9 are overlapping on the diffusion areas of the p-channel area 4 and the n-channel area 3. However, when such an overlap is abolished, a size of the conventional semiconductor cell becomes too large. Accordingly, it becomes difficult that the conventional semiconductor cells are integrated in a logic circuit with high density.

Referring to Figs. 2A, 2B, and 3, illustration will be made about a conventional semiconductor device. The conventional semiconductor device comprises three inverter cells 30 (one of which is illustrated in Fig. 1) to form a ring oscillator circuit, as shown in Fig. 3.

In the conventional semiconductor device, it is necessary that patterning spaces 10 are preserved at the both sides of the semiconductor device (namely, at both a lower side of a sheet of Fig. 2A or 2B and an upper side of a sheet of Fig. 2A or 2B). In other words, the second metal layer 2 is made to be extended up to the patterning spaces 10 at the both sides so as to electrically connect the inverter cells with each other. In this event, the length of wiring patterns between the semiconductor cells inevitably becomes large. Therefore, a size of the conventional semiconductor device becomes so large by the patterning spaces 10 which should be preserved at the both sides. Accordingly, it also becomes difficult that the conventional semiconductor devices are integrated in an IC or an LSI circuit with high density.

Referring now to Figs. 4 to 6, description will proceed to semiconductor cell and device according to an embodiment of this invention.

In Fig. 4, illustration is made about an inverter cell, a plurality of which are combined to form the semiconductor device according to the embodiment.

The inverter cell has a structure similar to that of the conventional inverter cell mentioned with reference to Fig. 1 except for the points described hereinunder. Similar portions are designated by like reference numerals.

In the illustrated inverter cell, the first metal layers 1b and 1c overlie whole areas of the p-channel and the n-channel areas 4 and 3. The contact holes 7 are provided to cover almost whole areas of the p-channel and the n-channel areas 4 and 3. As illustrated in Figs. 4 and 5, the first metal layers 1b and 1c and the second metal layers 2b and 2c have overlapping areas when considered in a vertical direction. The first and the second power supply terminals 8 and 9 consist of the overlapping areas, respectively.

With this structure, thick power supply lines (in other words, power supply lines having large cross

sections) which consist of the overlapping areas can be provided without occupying large areas in a plan view. The first metal layers 1a, 1b, and 1c and the second metal layers 2a, 2b, and 2c are electrically connected to each other by throughholes 6. Except for the first and the second power supply terminals 8 and 9, internal conductor patterns in the semiconductor cell are finished by the first metal layers 1a. Accordingly, electrical interconnection between the semiconductor cells can be readily achieved. Namely, the semiconductor cells are electrically connected to each other by the third metal layer 12 and the interconnecting area of the second metal layer 2a. Particularly, a conductor pattern of the second metal layer for signal transmission can be arranged within a space between the second metal layers 2b and 2c, as symbolized by a broken line block 13 in Fig. 5.

Referring to Figs. 6A and 6B, illustration will be made about a semiconductor device 40 according to the preferred embodiment of this invention. The semiconductor device 40 comprises three inverter cells (one of which is illustrated in Figs. 4 and 5) to form a ring oscillator circuit, as shown in Fig. 3.

In the illustrated semiconductor device 40, a conductor pattern arranging area 20 is defined between the power supply line 8 and the ground line 9. The conductor pattern arranging area 20 is formed by the above-mentioned spaces symbolized by the broken line block 13 in the three inverter cells. In the conductor pattern arranging area 20, the conductor pattern of the second metal layer 2a is arranged, as similarly mentioned before with respect to Fig. 5.

In the semiconductor device 40, for example, an interconnection between the semiconductor cells is accomplished by the second metal layer 2a. As a result, it becomes unnecessary that the second metal layers 2b and 2c are made to be extended up to the both sides of the power supply line 8 and the ground line 9. In other words, the semiconductor device 40 illustrated in Figs. 6A and 6B does not need any patterning spaces at the both sides. Therefore, the semiconductor device 40 does not become so large in size by such patterning spaces. In addition, as suggested in Fig. 6A, adjacent semiconductor devices 40' can be arranged at the both sides in the manner that the semiconductor device 40 has the power supply line 8 or the ground line 9 in common with the adjacent semiconductor devices 40' (in Fig. 6A, illustrated is only an adjacent semiconductor device 40' positioned at the upper side of a sheet of Fig. 6A). Accordingly, it becomes possible that the semiconductor devices 40 are integrated with high density in an IC or an LSI circuit.

Besides, the semiconductor device 40 is electrically connected to the adjacent semiconductor devices 40' by the third metal layer 12, as depicted by a broken line in Fig. 6A. Furthermore, each of input and output terminals of the semiconductor cell can be formed at an optional point in the first metal layers 1b and 1c. Consequently, the interconnection between the semiconductor cells can be freely laid out.

As mentioned above, according to the present invention, a parasitic resistance in the diffusion areas is considerably decreased. An operation speed of the semiconductor cell can be so improved.

In order to confirm characteristics of the semiconductor device 40, a simulation test was carried out by the inventor of the present invention.

In the simulation test, a delay time was measured in connection with the semiconductor device 40 which comprises three chained inverters. As a result, the delay time in the semiconductor device 40 was 0.9 to 0.95 times less than that of the conventional semiconductor device. Namely, decrease of the delay time was approximately five to ten percentages. In addition, the semiconductor devices 40 can be integrated with high density in an IC or an LSI circuit, since wiring spaces for power supply or signal lines are considerably reduced in the semiconductor devices 40.

In order to confirm this advantage, two adders were fabricated. One was laid out by the use of the semiconductor device 40 while another was laid out by the use of the conventional semiconductor device. As a result of comparison of transistor density between the two adders, the adder laid out by the use of the semiconductor devices 40 could be fabricated with a transistor density about 1.5 times higher than that laid out by the conventional semiconductor devices.

While this invention has thus far been described in specific conjunction with the preferred embodiment thereof, it will now be readily possible for one skilled in the art to put this invention into effect in various other manners. For example, the semiconductor device is not restricted to such one as comprising CMOS. The semiconductor device of the present invention may comprise BiCMOS, nMOS, BinMOS, or the like. Furthermore, the connecting portion comprises a plurality of contact holes in the preferred embodiment. The connecting portion may comprise a contact hole which covers almost whole of the diffusion area.

Claims

1. A semiconductor device (40), comprising:

a plurality of semiconductor cells (30) each of which includes:

a diffusion area (3, 4); a first metal layer (1a, 1b, 1c) which forms internal conductor

patterns; and connecting means (7) for connecting said diffusion area (3, 4) to said first metal layer (1a, 1b, 1c);

a second metal layer (2a, 2b, 2c);

a third metal layer (12);

first and second power supply lines (8 and 9);

characterized in that:

said first metal layer (1b, 1c) overlies whole of said diffusion area (3, 4);

said connecting means (7) cover almost whole of said diffusion area (3, 4); and that:

said second metal layer (2a, 2b, 2c) has an interconnecting area positioned above said semiconductor cells (30);

said first and said second metal layers (1b, 1c, 2b, 2c) having an overlapping area overlapping on each other;

each of said first and said second power supply lines (8 and 9) consisting of said overlapping area; and

said semiconductor cells (30) being electrically connected to each other by said third metal layer (12) and said interconnecting area of said second metal layer (2a, 2b, 2c).

2. A semiconductor device (40) as claimed in Claim 1, characterized in that each of said semiconductor cells (30) is made of complementary metal oxide semiconductor transistors, said diffusion area (3, 4) comprising a p-channel area (4) and an n-channel area (3).

3. A semiconductor device (40) as claimed in Claim 1, characterized in that said connecting means (7) comprise a plurality of contacts.

4. A semiconductor device (40) as claimed in Claim 1, characterized in that said connecting means (7) comprise a contact covering almost whole of said diffusion area (3, 4).

5. A semiconductor cell (30), comprising:

a diffusion area (3, 4); a first metal layer (1a, 1b, 1c) which forms internal conductor patterns; and connecting means (7) for connecting said diffusion area (3, 4) to said first metal layer (1a, 1b, 1c);

a second metal layer (2a, 2b, 2c);

first and second power supply terminals (8 and 9);

characterized in that:

said first metal layer (1b, 1c) overlies whole of said diffusion area (3, 4) and that said connecting means (7) cover almost whole of said diffusion area (3, 4);

said first and said second metal layers (1b, 1c, 2b, 2c) having an overlapping area overlapping on each other; and

each of said first and said second power supply terminals (8 and 9) consisting of said overlapping area.

6. A semiconductor device (40), comprising:

a plurality of semiconductor cells (30) each of which includes:

a diffusion area (3, 4); a first metal layer (1a, 1b, 1c) which forms internal conductor patterns; and connecting means (7) for connecting said diffusion area (3, 4) to said first metal layer (1a, 1b, 1c);

a second metal layer (2a, 2b, 2c);

first and second power supply lines (8 and 9);

characterized in that:

said first metal layer (1b, 1c) overlies whole of said diffusion area (3, 4);

said connecting means (7) cover almost whole of said diffusion area (3, 4); and that:

said second metal layer (2a, 2b, 2c) has an interconnecting area positioned above said semiconductor cells (30);

said first and said second metal layers (1b, 1c, 2b, 2c) having an overlapping area overlapping on each other;

each of said first and said second power supply lines (8 and 9) consisting of said overlapping area; and

said semiconductor cells (30) being electrically connected to each other by said interconnecting area of said second metal layer (2a, 2b, 2c).

7. A semiconductor device (40) as claimed in Claim 6, further comprising a third metal layer (12), characterized in that said semiconductor cells (30) are electrically connected to each other by said third metal layer (12) in addition to said interconnecting area of said second metal layer (2a, 2b, 2c).

8. A semiconductor integrated circuit, comprising:

a plurality of semiconductor devices (40, 40') each of which has:

a plurality of semiconductor cells (30) each of which includes:

a diffusion area (3, 4); a first metal layer (1a, 1b, 1c) which forms internal conductor patterns; and connecting means (7) for connecting said diffusion area (3, 4) to said first metal layer (1a, 1b, 1c);

a second metal layer (2a, 2b, 2c);

a third metal layer (12);

first and second power supply lines (8 and 9);

characterized in that:

said first metal layer (1b, 1c) overlies whole of said diffusion area (3, 4);

said connecting means (7) cover almost whole of said diffusion area (3, 4); and that:

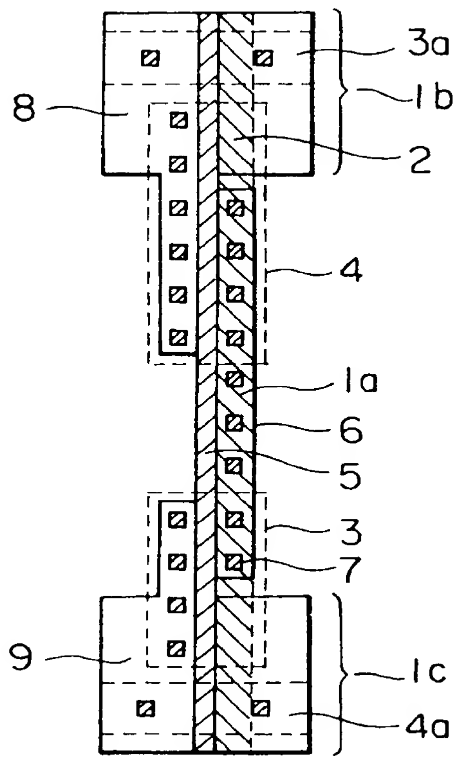
said second metal layer (2a, 2b, 2c) has an interconnecting area positioned above said semiconductor cells (30);

said first and said second metal layers (1b, 1c, 2b, 2c) having an overlapping area overlapping on each other;

each of said first and said second power supply lines (8 and 9) consisting of said overlapping area; and

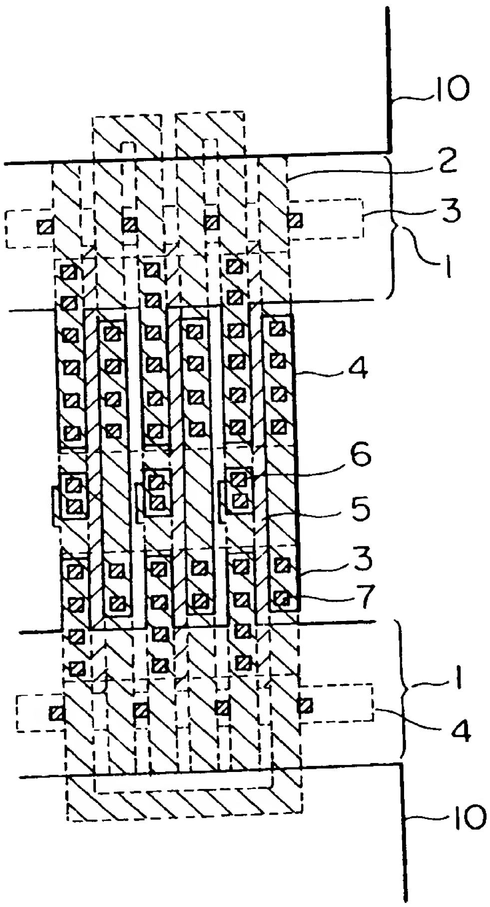
said semiconductor cells (30) being electrically connected to each other by said third metal layer (12) and said interconnecting area of said second metal layer (2a, 2b, 2c); and

said semiconductor devices (40, 40') being electrically connected to each other by said third metal layer (12).



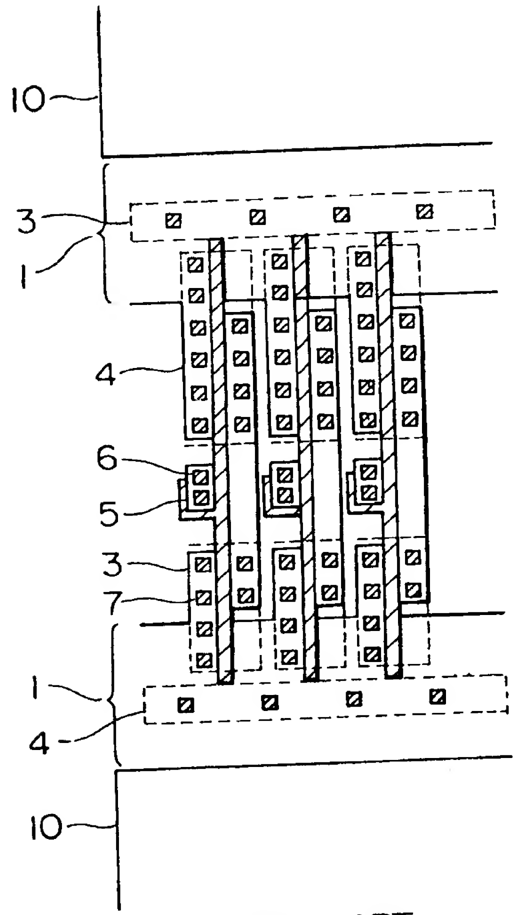
PRIOR ART

FIG. 1



PRIOR ART

FIG. 2A



PRIOR ART

FIG. 2B

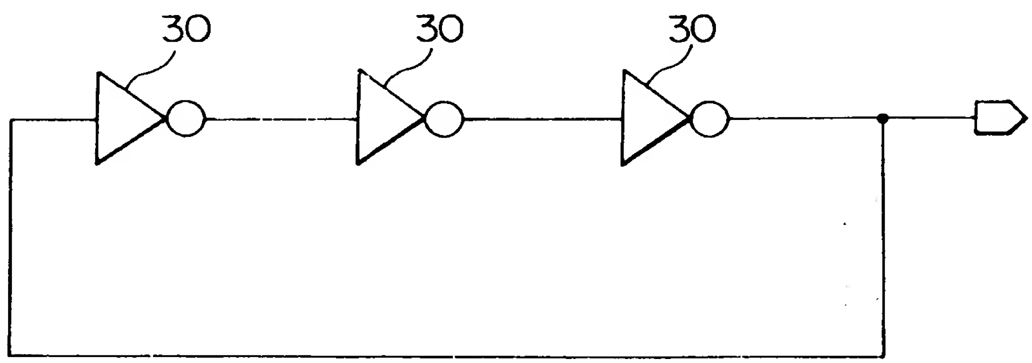


FIG. 3

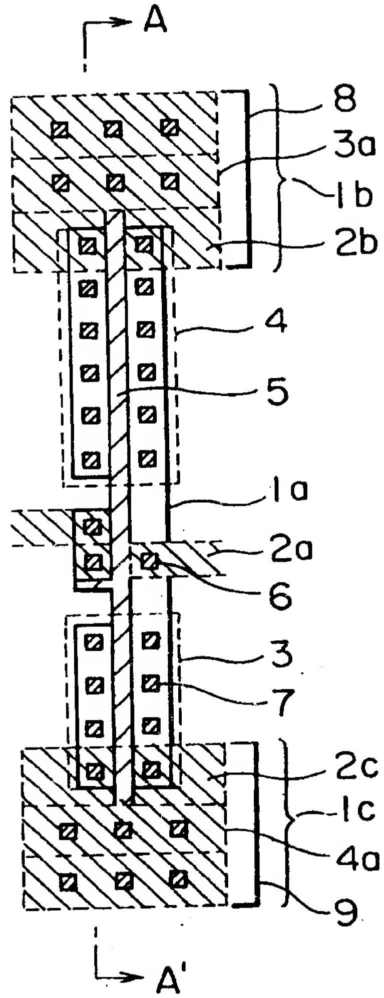


FIG. 4

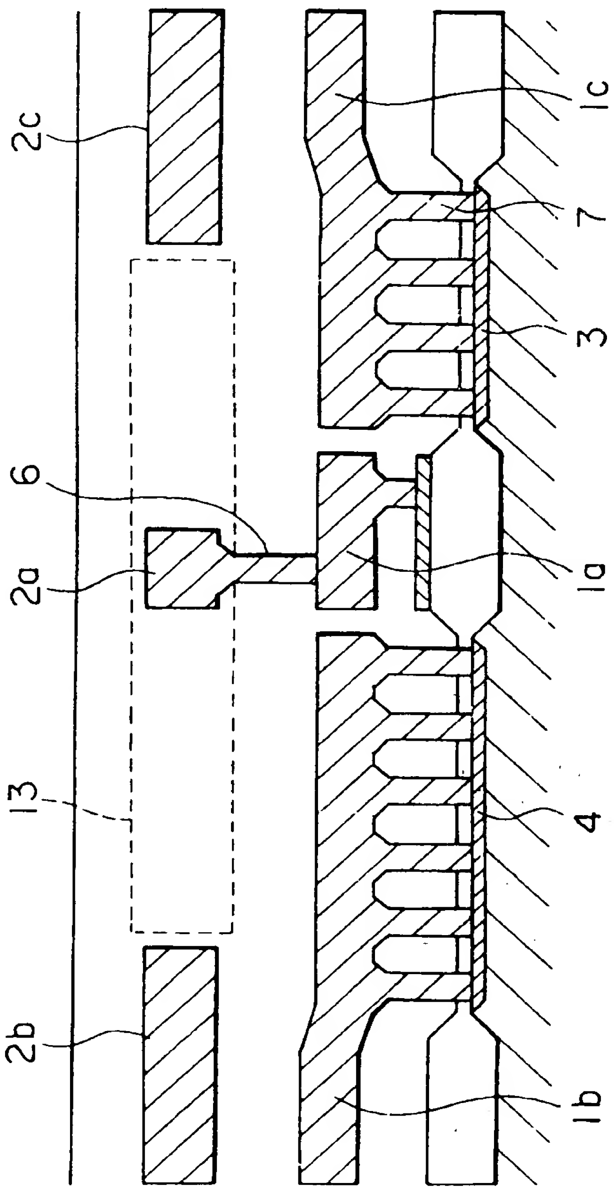


FIG. 5

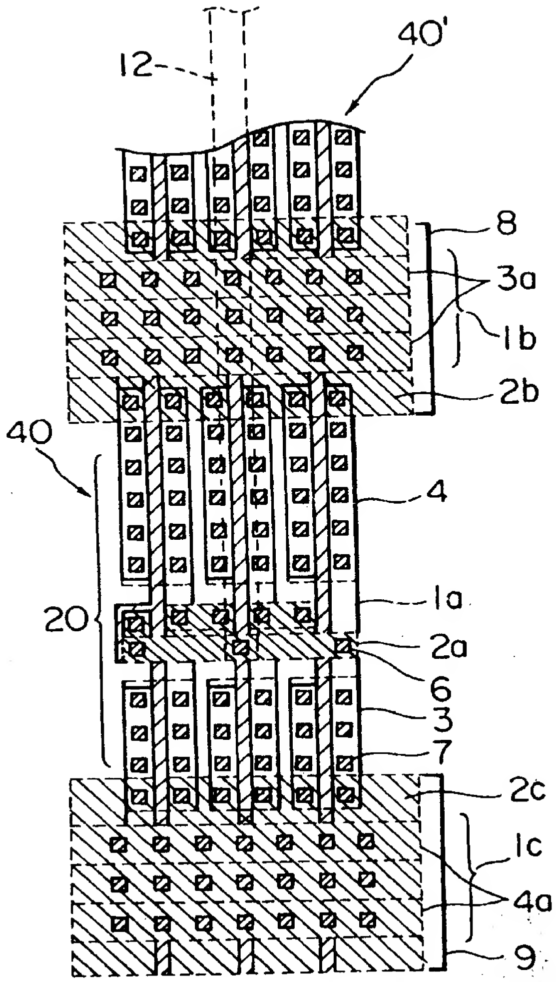


FIG. 6A

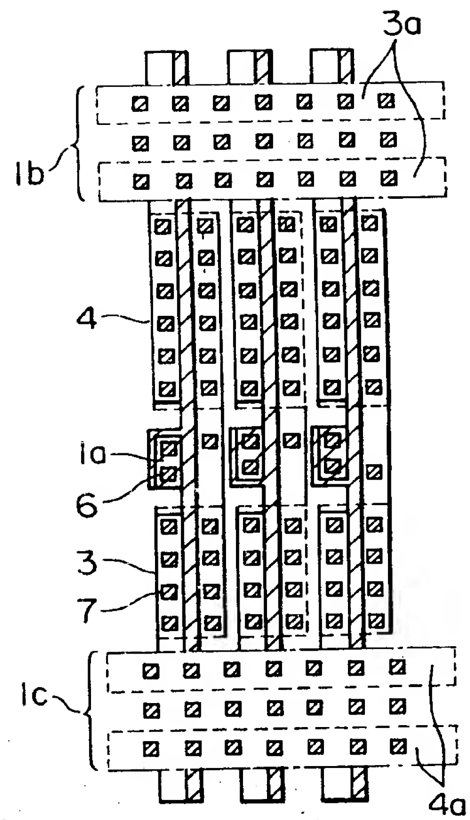


FIG. 6B